

CLAIMS

What is claimed is:

- 1 1. A microelectronic component assembly, comprising:
2 a first substrate having at least one contact;
3 a second substrate having at least one contact;
4 at least one solder ball extending between said at least one first substrate contact
5 and said at least one second substrate contact, wherein said at least one solder ball is
6 attached to said at least one first substrate contact; and
7 a compression mechanism for imparting pressure between said first substrate and
8 said second substrate.

- 1 2. The microelectronic component assembly of claim 1, wherein said first
2 substrate comprises a microelectronic device package.

- 1 3. The microelectronic component assembly of claim 1, wherein said first
2 substrate comprises a carrier substrate.

- 1 4. The microelectronic component assembly of claim 1, wherein said first
2 substrate comprises a microelectronic device.

1 5. The microelectronic component assembly of claim 1, wherein said at least
2 one second substrate contact comprises a recess defined by at least one sidewall
3 extending into said second substrate.

1 6. The microelectronic component assembly of claim 5, wherein said at least
2 one recessed second substrate contact includes a width which is substantially the same as
3 a diameter of said solder ball.

1 7. The microelectronic component assembly of claim 5, wherein said at least
2 one recessed second substrate contact has a semispherical surface which is substantially
3 the same radius as a radius of said solder ball.

1 8. A method of fabricating a microelectronic component assembly,
2 comprising:
3 providing a first substrate having at least one contact;
4 providing a second substrate having at least one contact;
5 attaching at least one solder ball on said at least one first substrate contact;
6 aligning said at least one solder ball with said at least one second substrate
7 contact; and
8 imparting pressure between said first substrate and said second substrate.

1 9. The method of claim 8, wherein providing said first substrate comprises
2 providing a microelectronic device package.

1 10. The method of claim 8, wherein providing said first substrate comprises
2 providing a carrier substrate.

1 11. The method of claim 8, wherein providing said first substrate comprises
2 providing a microelectronic device.

1 12. A microelectronic component assembly, comprising:
2 a first substrate having a first surface and a second surface, wherein said first
3 substrate first surface includes at least one contact;
4 a second substrate having a first surface and a second surface; wherein said
5 second substrate first surface includes at least one contact;
6 at least one solder ball extending between said at least one first substrate first
7 surface contact and said at least one second substrate first surface contact, wherein said at
8 least one solder ball is attached to one of said at least one first substrate first surface
9 contact and said at least one second substrate first surface contact; and
10 a support structure for imparting pressure between said first substrate and said
11 second substrate.

4 a backing plate abutting said second substrate second surface;
5 a thermal plate extending over said frame and adjacent said first substrate second
6 surface;
7 a plurality of retention devices extending through said backing plate, said frame;
8 and the thermal plate; and
9 a resilient spacer extending between said thermal plate and said interposer
10 substrate.

1 17. A method of fabricating a microelectronic component assembly,
2 comprising:
3 providing a first substrate having a first surface and a second surface, wherein
4 said first substrate first surface includes at least one contact;
5 providing a second substrate having a first surface and a second surface; wherein
6 said second substrate first surface includes at least one contact;
7 attaching at least one solder ball to one of said at least one first substrate first
8 surface contact and said at least one second substrate first surface contact
9 aligning said at least one first substrate first surface contact with said at least one
10 second substrate first surface contact; and
11 imparting pressure between said first substrate and said second substrate with a
12 support structure.

1 20. The method of claim 18, wherein providing said substrate comprises
2 providing a microelectronic device package including a microelectronic device attached
3 to and in electrical contact with a first surface of an interposer substrate, and wherein
4 said at least one substrate first surface contact comprises at least one contact on a
5 second surface of said interposer substrate.

1 21. The method of claim 20, further including disposing a thermal interface
2 between a back surface of said microelectronic device and said thermal plate.

1 22. The method of claim 20, further including disposing a resilient spacer
2 between said interposer substrate and said thermal plate.

1 23. A substrate contact for forming a non-reflow electrical contact with a
2 solder ball, comprising:
3 a recess defined in a substrate by at least one surface extending into said substrate;
4 and
5 a conductive material layered in said recess.

1 24. The substrate contact of claim 23, wherein said surface comprises at least
2 one substantially vertical sidewall.

1 25. The substrate contact of claim 24, further including a width of said recess,
2 including said layered conductive material, which is substantially the same as a diameter
3 of said solder ball.

1 26. The substrate contact of claim 23, wherein said at least one surface
2 extending into said substrate comprises a semispherical recess, wherein an upper surface
3 of said conductive material has substantially the same radius as a radius of said solder
4 ball.

1 27. The substrate contact of claim 25, further including a resilient material
2 disposed between said substrate and said conductive material layer.

1 28. A substrate contact for forming a non-reflow electrical contact with a
2 solder ball, comprising:
3 a recess define in a substrate by at least one surface extending into said substrate;
4 and
5 a conductive material layered over said recess forming a void in said recess.